

REMARKS

In the present Amendment, Applicants have canceled claims 1, 6, and 9, without prejudice or disclaimer of the subject matter thereof. Applicants have amended claims 2-5, 7-8, 10-12, and 16 to more appropriately define the invention. Applicants have also added new claims 36-38 to protect additional aspects of the invention. No new matter has been added. Upon entry of this Amendment, claims 2-5, 7-8, and 10-38 are pending.

In the Office Action, the Examiner rejected claims 1-6, 8-11, and 16-35 under 35 U.S.C. §102(e) as being anticipated by Ker et al. (U.S. Patent No. 6,521,952). The Examiner also objected to claims 7 and 12-15 as being dependent upon a rejected base claim, but mentioned that they would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Applicants appreciate the indication of allowable subject matter. Applicants have rewritten claim 7 in independent form to include all the recitations of base claim 1 and intervening claim 6, and have rewritten claim 12 in independent forms to include all the recitations of base claim 1. As indicated by the Examiner, claim 7 as amended is allowable. Applicants respectfully deem that claim 12 as so rewritten is patentable, without the need to also include the recitations of claim 11, as explained more fully below. Applicants have also canceled claims 1, 6, and 9, and as a result, the rejection of these claims is rendered moot.

Applicants respectfully traverse the rejection of claims 2-5, 8, 10-11, and 16-35 under 35 U.S.C. § 102(e).

In order to properly anticipate Applicants' claimed invention under 35 U.S.C. §102, each and every element of the claim in issue must be found, "either expressly or

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inherently described, in a single prior art reference." "The identical invention must be shown in as complete detail as is contained in the . . . claim. *Richardson v. Suzuki Motor Co.*, 868 F.2d 1226, 1236, 9 USPQ2d 1913, 1920 (Fed. Cir. 1989)." See M.P.E.P. § 2131, 8th ed., 2001.

The present invention is in general directed to an electrostatic discharge (ESD) protection circuit incorporating a silicon controlled rectifier (SCR) in a silicon-on-insulator (SOI) semiconductor device. Particularly, amended independent claim 5 recites, among others, "a layer of silicon material, . . . including a first p-type portion, a first n-type portion contiguous with the first p-type portion, a second p-type portion contiguous with the first n-type portion, a second n-type portion contiguous with the second p-type portion, a third p-type portion contiguous with the second n-type portion, a third n-type portion contiguous with the third p-type portion, and a fourth n-type portion formed entirely in the second p-type portion and spaced apart from the first n-type portion."

Ker et al., discloses a method of forming a silicon controlled rectifier devices in silicon-on-insulator (SOI) CMOS processes. Referring to Fig. 5a, Ker et al. describes that "[a] P-type well (P2) 104 is provided, . . . [an] N-type well (N1) 106 is disposed adjacent to the P-type well (P2) 104 . . . [a] P⁺ region (P1) 108 is implanted into the N-type well 106, . . . [an] N⁺ region (N4) 110 is implanted into the N-type well (N1) 106 . . . [a] heavily doped N-type region (N3) 112 lies adjacent to the N-type well (N1) 106 and P-type well (P2) 104, and forms a new P2-N3 junction instead of the P2-N1 junction . . . [a] heavily doped N-type region (N2) 114 is provided in the P-type well (P2) 104 . . . , [and a] heavily doped P-type region (P3) 116 is provided in the P-type well (P2) 104."

Col. 5, lines 33-60.

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With regard to claim 5, the Examiner alleged that "the second p-type portion, (Figure 5a #104), additionally includes a fourth n-type portion, (Figure 5a #112), spaced apart from the first n-type portion." Office Action, page 3. Applicants note that, as shown in Fig. 5a of Ker et al., N-type region 112, allegedly corresponding to Applicants' claimed fourth n-type portion, is not "formed entirely in" P-well 104, allegedly corresponding to Applicants' claimed second p-type portion. Instead, "heavily doped N-type region (N3) 112 lies adjacent to the N-type well (N1) 106 and P-type well (P2) 104." Col. 5, lines 49-51. Therefore, Ker et al. fails to teach "a fourth n-type portion formed entirely in the second p-type portion and spaced apart from the first n-type portion," as recited in claim 5.

Similarly, amended claim 12 recites, among others, "a fourth p-type portion formed entirely in the second n-type portion and spaced apart from the third p-type portion." Ker et al. at least fails to teach this feature.

As a result, claims 5 and 12 are allowable over Ker et al. under 35 U.S.C. § 102(e), and claims 2-4, 8, 10-11, 13-16, and 36-38, which depend from independent claims 5 and 12, are also allowable over Ker et al., at least because of their dependencies from an allowable base claim.

Moreover, independent claim 17 recites, among other things, "an n-type MOS transistor having a gate, a drain region, and a source region formed over the isolation layer; and a p-type MOS transistor having a gate, a drain region, and a source region formed over the isolation layer and contiguous with the n-type MOS transistor, wherein the n-type MOS transistor and the p-type MOS transistor form a rectifier to provide electrostatic discharge protection."

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The Examiner alleged in the Office Action that Ker et al. teaches "an n-type MOS transistor, (Figure 5a #123), . . . and a p-type MOS transistor, (Figure 5a #124), having a gate, (Figure 5a #124), a drain region and a source region, (Figure 5a #112 & 108), formed over the isolation layer, (Figure 5a #128), and contiguous with the n-type MOS transistor, (Figure 5a #123)." Office Action, pages 4-5. Applicants respectfully disagree.

Applicants submit that element 124 of Ker et al. is "dummy gate (G1)," *not* a p-type MOS transistor. Col. 6, line 2. Also, according to Ker et al., element 108 is a "P⁺ region," while element 112 is a "heavily doped N-type region." Col. 5, lines 41-49. Therefore, element 108 and element 112 *cannot* form a drain region and a source region of a p-type MOS transistor, because the drain region and the source region of a p-type MOS transistor should be both p-type diffusion regions. Referring to Fig. 5a, Ker et al. does not teach a p-type MOS transistor that is "formed over the isolation layer and contiguous with" NMOS 123, allegedly corresponding to Applicants' claimed n-type MOS transistor.

As a result, Ker et al. fails to teach each and every element of claim 17. Particularly, Ker et al. fails to teach at least "a p-type MOS transistor having a gate, a drain region, and a source region formed over the isolation layer and contiguous with the n-type MOS transistor," as recited in claim 17. Therefore, claim 17 is allowable over Ker et al. under 35 U.S.C. § 102(e), and claims 18-32, which depend from claim 17, are also allowable at least because of their dependency from an allowable base claim.

Finally, claim 33 recites, among other things, "providing an n-type MOS transistor . . . providing a p-type MOS transistor . . . contiguous with the n-type MOS transistor."

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For similar reasons as set forth above, Ker et al. at least fails to teach these features of claim 33. Therefore, claim 33 is allowable over Ker et al., and claims 34 and 35, which depend from claim 33, are also allowable over Ker et al. at least because of their dependency from an allowable base claim.

In view of the foregoing amendments and remarks, Applicants respectfully request the reconsideration and reexamination of this application and the timely allowance of pending claims 2-5, 7-8, and 10-38.

Please grant any extensions of time required to enter this response and charge any additional required fees to our deposit account 06-0916.

Respectfully submitted,

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